Introduction to Prototyping Using PolyMUMPs

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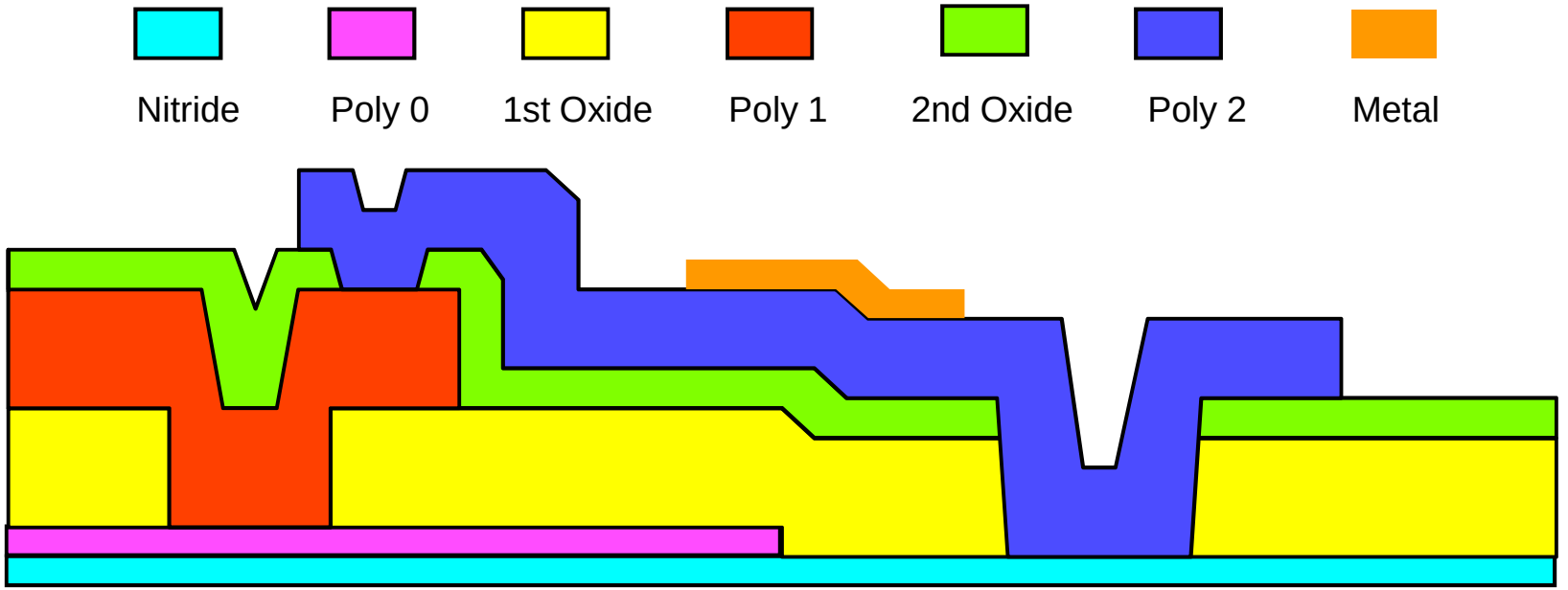
Basado en una presentación de Steve Wilcenski, MEMSCAP Inc.

About MUMPs®

- Multi-user Manufacturing Process, allows inexpensive access to silicon by sharing design on the same wafer
- Company MEMSCAP offers three processes: PolyMUMPS, SOIMUMPS, MetalMUMPS. Available through EuropractICe
- The baseline process of the the MUMPs® program is the 3-layer polysilicon surface micromachining process known as PolyMUMPs
- PolyMUMPS developed in Berkeley BSAC in the 80s
- The basic process includes 8* lithography levels, and 7 physical layers
  - 2 mechanical and 1 electrical layer of polysilicon
  - 2 sacrificial layers
  - 1 electrical conduction
  - 1 electrical isolation layer

PolyMUMPs Process



Seven Physical Layers

- Nitride
  - **Isolation between substrate and electrical surface layers**
- Poly zero
  - **Electrical poly layer for ground plane or electrode formation. Below the first mechanical layer**
- First oxide
  - **First sacrificial oxide layer, providing gap between poly1 and substrate/nitride**
- Poly 1
  - **First mechanical layer**
- Second oxide
  - **Second sacrificial oxide layer, provides gap between second and first polysilicon**
- Poly 2
  - **Second mechanical layer**
- Metal
  - **Provides electrical connection to package**

Eight Lithography Levels

- POLY ZERO
  - **Defines the polysilicon zero features**
- ANCHOR 1
  - **Opens points-of-contact between first polysilicon and substrate (nitride or poly 0)**
- DIMPLE
  - **Generates 'bumps' in under-surface of poly 1 to minimize stiction**
- POLY 1
  - **Defines first polysilicon features**
- POLY1_POLY2_VIA
  - **Opens points-of-contact between first and second polysilicon**
- ANCHOR 2
  - **Opens points-of-contact between second polysilicon and substrate/nitride**
- POLY 2
  - **Defines second polysilicon features**
- METAL
  - **Defines location of metal features**

Common Layout Terminology

- Layer
  - a physical layer of material deposited during the fabrication process
    - Always represented in mixed-case letters
- LEVEL
  - a lithographic level used to pattern a physical layer. It may or may not correspond with a physical layer
    - e.g. poly1= POLY1, but Second oxide is patterned by both ANCHOR2 and POLY1_POLY2_VIA
    - Always represented in CAPITAL letters

Common Layout Terminology

- Dimples
  - small, shallow features in the underside of the lower polysilicon layer to minimize the area of contact between the polysilicon and the substrate
- CVD: Chemical Vapor Deposition
  - a method of depositing layers of material through the interaction of gases at low vacuum and increased temperature
    - A CVD deposition is generally conformal - follows closely the underlying topography

Common Layout Terminology

- PSG: Phospho-silicate-glass
  - a phosphorous containing silicon dioxide layer generated by CVD and used for its fast etching properties
- Sacrificial oxide
  - a layer of fast etching silicon dioxide used to define the separation between the mechanical layers and the substrate
- RIE: Reactive Ion Etching
  - a dry physical or chemical etching method which removes specific material through the interaction of gas and plasma with the wafer surface

Common Layout Terminology

- Stringer
  - a ribbon of material left behind after an RIE etch step. Generally created at a topographic edge
- Lift-off
  - a method of depositing metal which uses a polymer template. The sidewall profile of the polymer is defined such that the continuity of the deposited metal is interrupted by the step, and subsequent insertion into a solvent bath removes the polymer layer and the metal residing upon it

Common Layout Terminology

- Release
  - the last step of the process where the sacrificial layers are removed by submersion into HF
- Stiction
  - the sticking effect between polysilicon and the substrate which occurs during the removal of the sacrificial oxide. Many attempts to limit stiction, including dimples, special release chemicals and processes, are tried, some successfully

Why Design Rules?

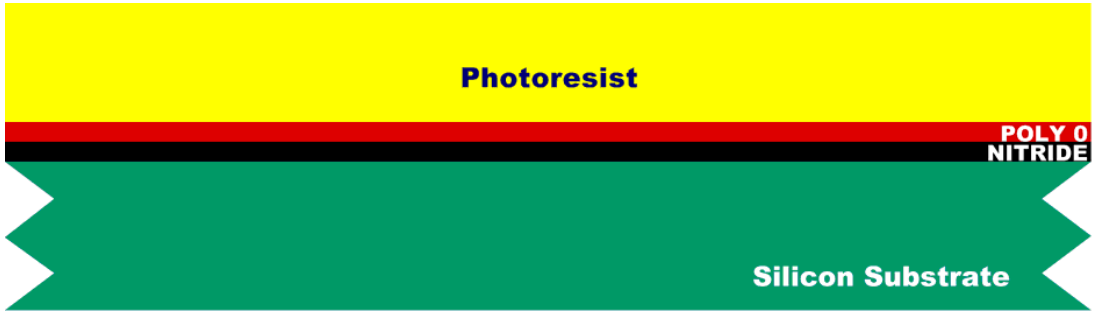
- Design rules define configurations that are allowed and those which are not
- Determined by normal manufacturing limitations (process window)
  - Minimum resolution of the lithography system
  - Alignment between levels
  - Topography effects of multiple layers
  - Etch requirements
    - Selectivity between materials
    - Etch rates

MUMPs® Design Rules

- Most process rules in MUMPs® are "advisory"
  - warn of possible negative interactions
  - must be taken in context of the design
  - violations are at user's risk
- A few rules are mandatory and may not be violated
  - Minimum line and spaces - determined by lithographic resolution
  - A few interlevel interactions - required by process window

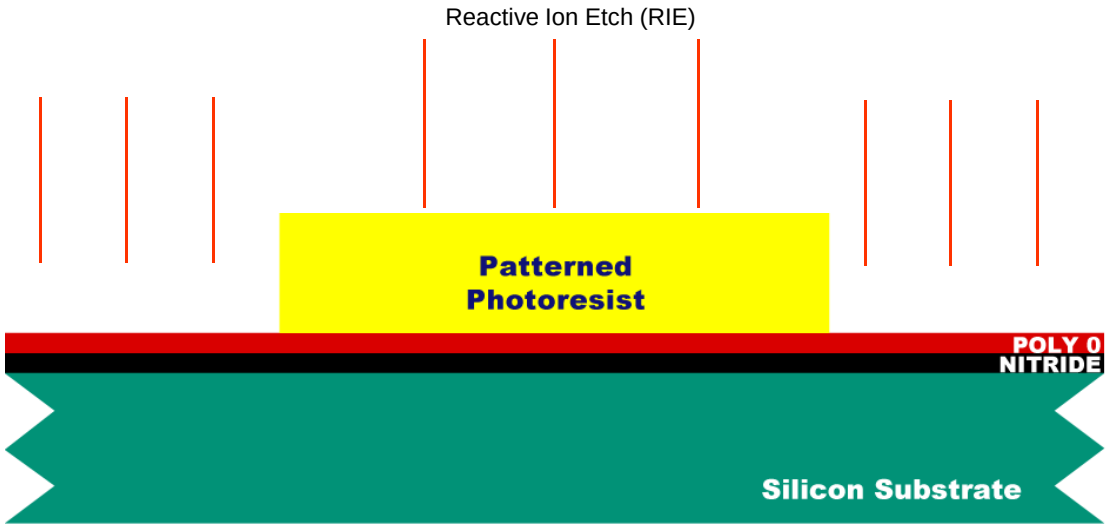
PolyMUMPs Process

- Heavily doped N+ layer diffused into surface of starting wafer
  - Minimizes charge feed-through on wafer surface
- Low stress nitride and poly zero layers are deposited (blanket). Wafer is spin coated with photoresist.



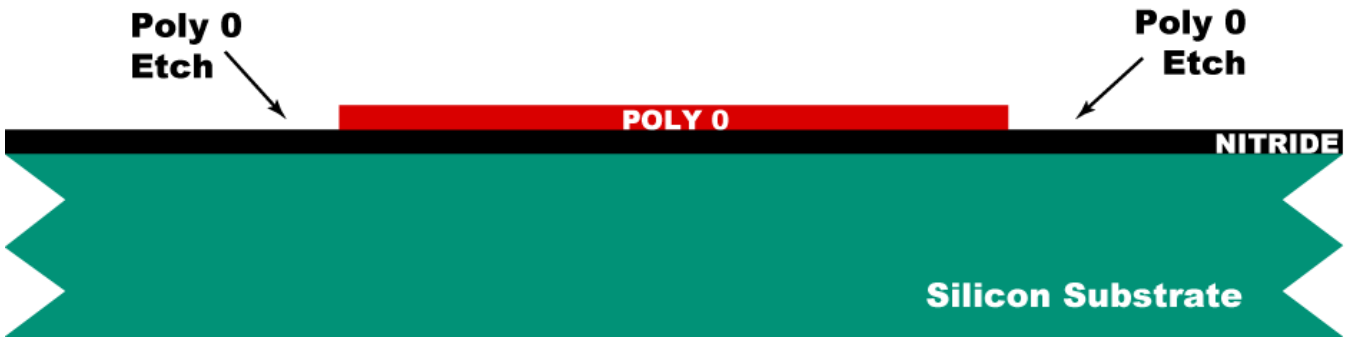
PolyMUMPs Process

- The photoresist is exposed using the first mask level (POLY0) and the image is developed.
- The exposed polysilicon is then removed by RIE etching, transferring the POLY0 pattern onto the wafer.



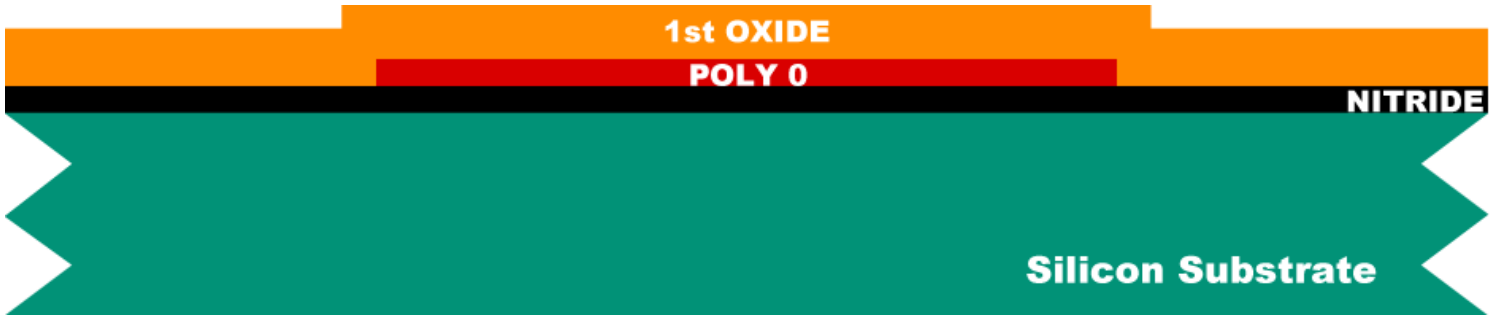
PolyMUMPs Process

- The photoresist is stripped in solvent after etch.



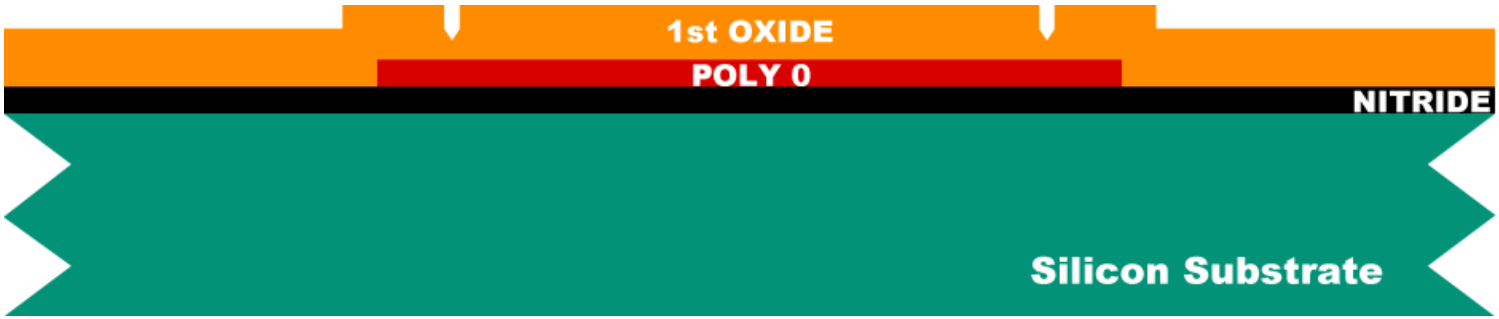
PolyMUMPs Process

- The first oxide layer (2.0 µm) is deposited on the wafer by low temperature CVD.



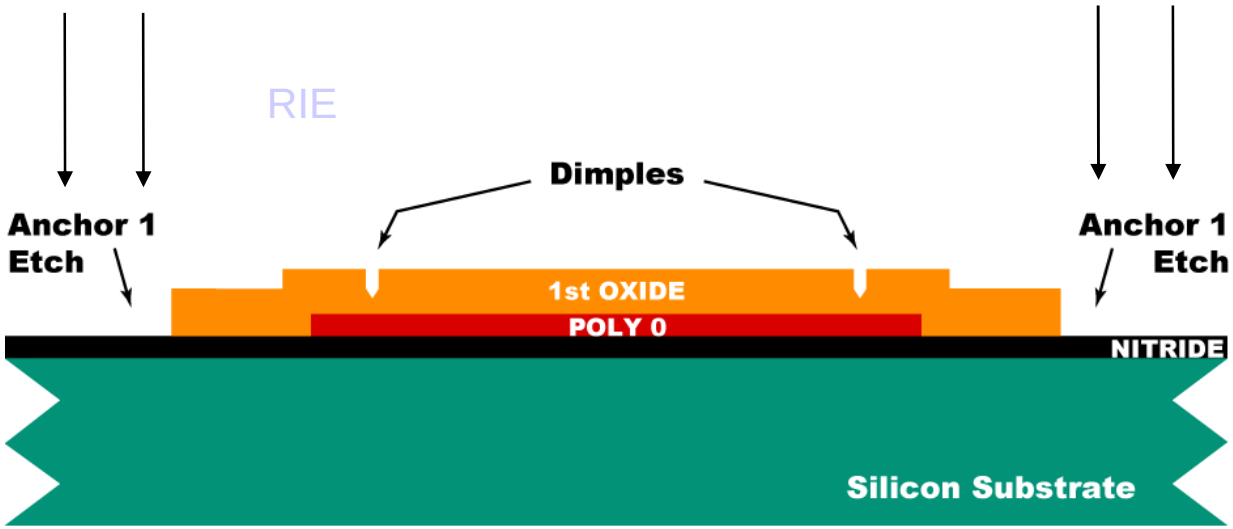
PolyMUMPs Process

- The wafer is coated with photoresist and second mask level (DIMPLE) is exposed and developed.



PolyMUMPs Process

- The dimple photoresist is stripped and a new layer of photoresist is applied for the third mask level (ANCHOR1). The first oxide is patterned and then processed through RIE to remove the oxide from the anchor area.

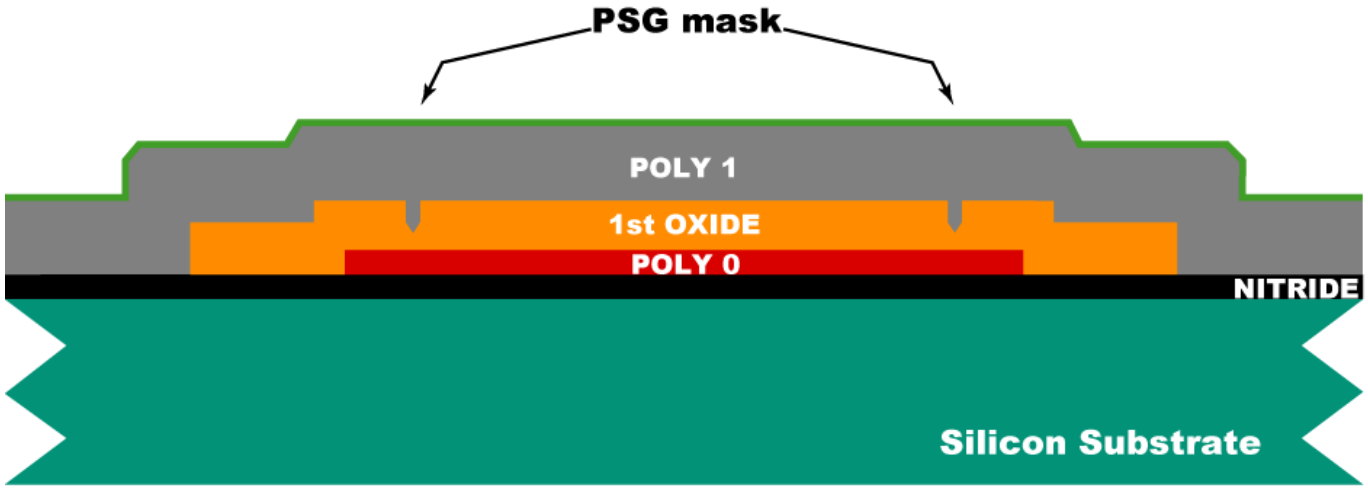


PolyMUMPs Process

- The photoresist is stripped in a solvent bath and the wafer is ready for poly 1 processing.
- ANCHOR1 defined where poly 1 will be attached to the substrate, and the thickness of the first oxide defines how far above the substrate (either nitride or poly0) poly 1 will sit after release.

PolyMUMPs Process

- After the wafer is cleaned, the first polysilicon layer is deposited by LPCVD. An additional thin PSG layer is deposited on top of the poly 1 and the wafer is annealed at high temperature to reduce the residual stress and dope the poly 1.



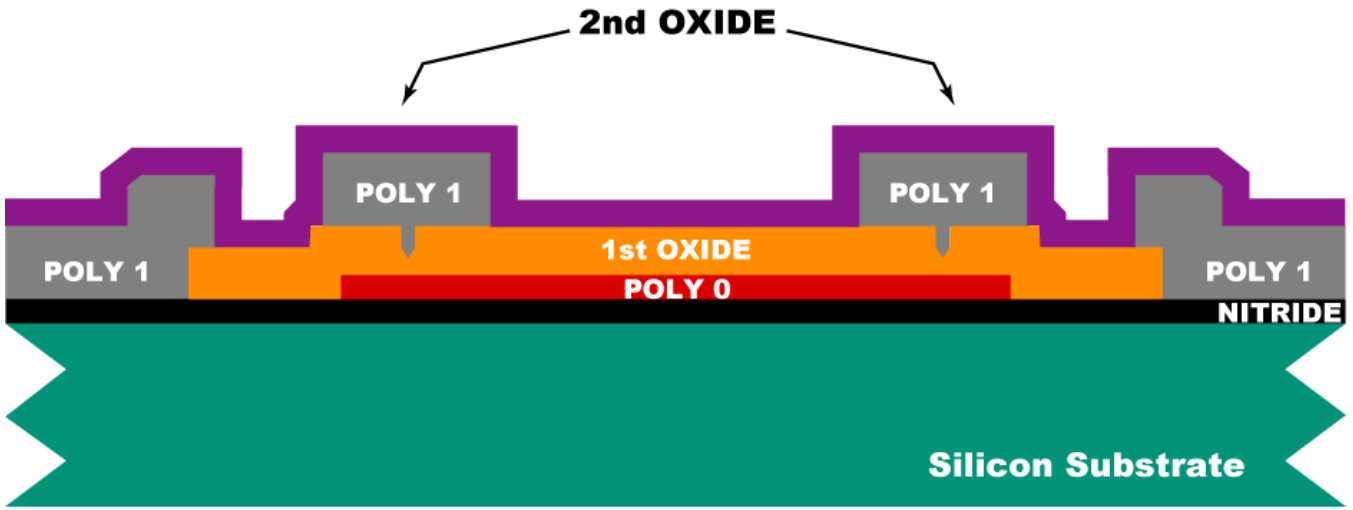
PolyMUMPs Process

- The wafer is coated with photoresist and the fourth mask (POLY1) is patterned. The wafer is RIE etched, stopping on the first oxide, using both the photoresist and thin PSG (top) layer as masks for the poly 1 layer.

Etch

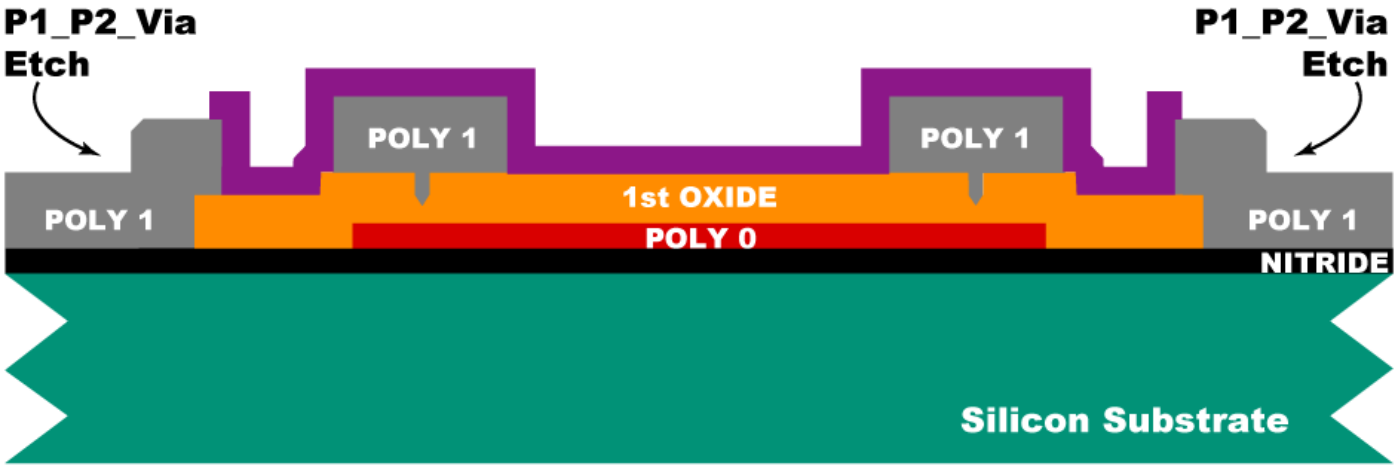
PolyMUMPs Process

- The second oxide layer (0.75 μm) is deposited by low temperature CVD, conformally coating the topography on the wafer and defining the separation of the first poly layer from the second polysilicon.



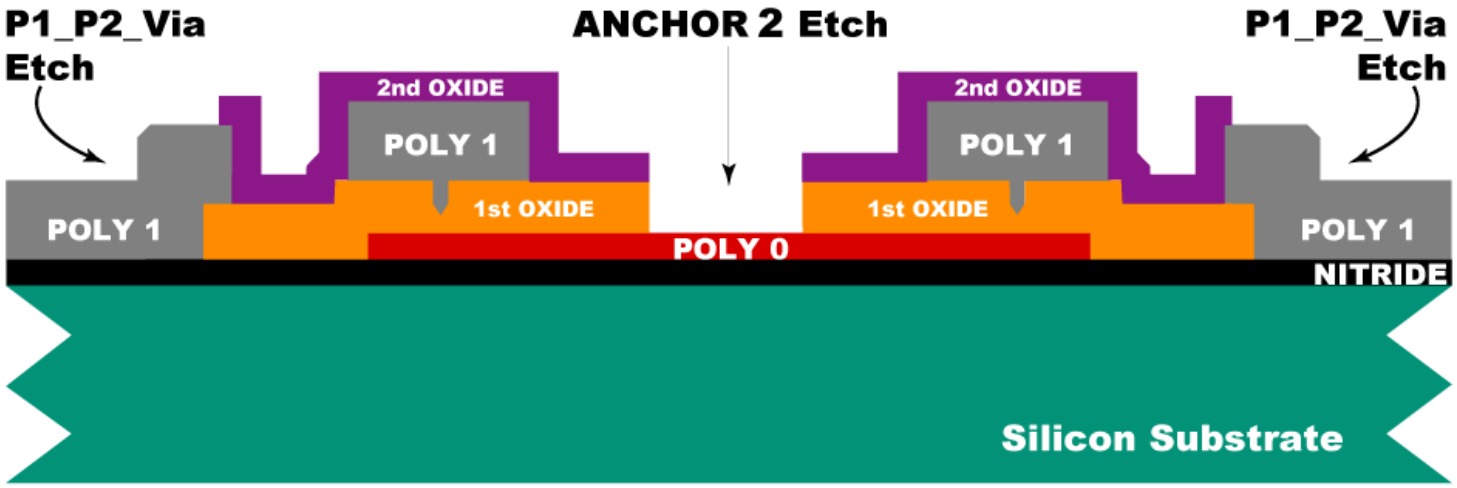
PolyMUMPs Process

- The wafer is coated with photoresist and the fifth mask (POLY1_POLY2_VIA) is patterned and RIE etched. This defined the contact regions between poly 1 and poly 2.



PolyMUMPs Process

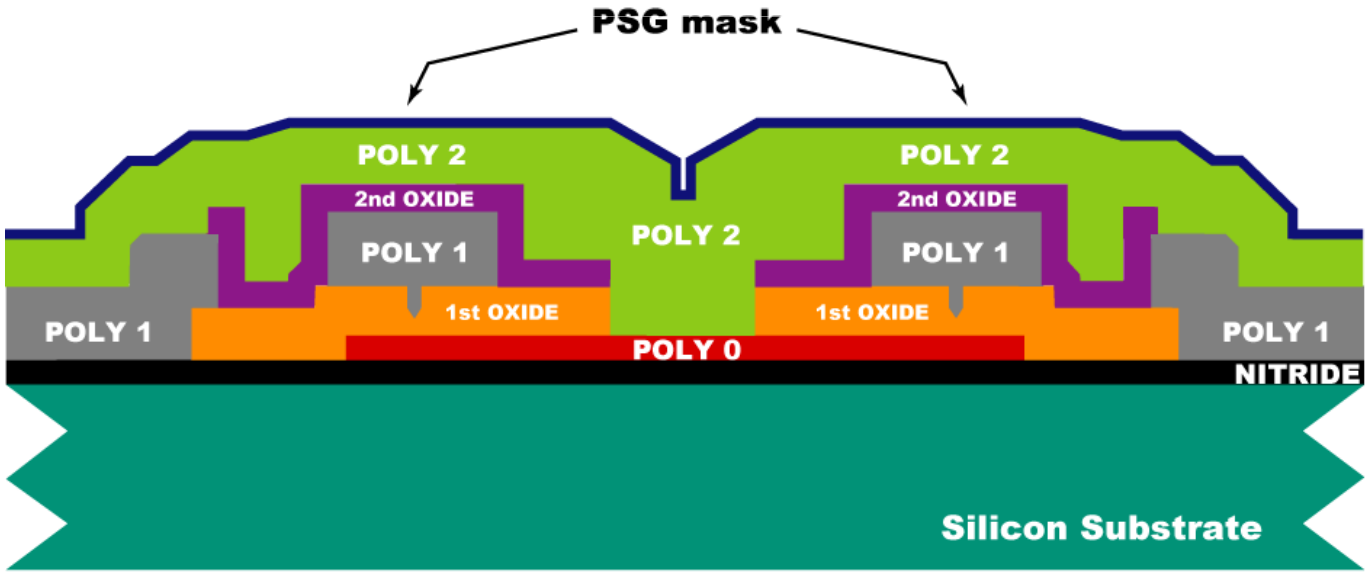
- The photoresist is stripped and the wafer is recoated. The sixth mask (ANCHOR2) is patterned and both first oxide and second oxide are etched in one step. This defines the region where poly2 will contact the substrate (either nitride or poly0).



Silicon Substrate

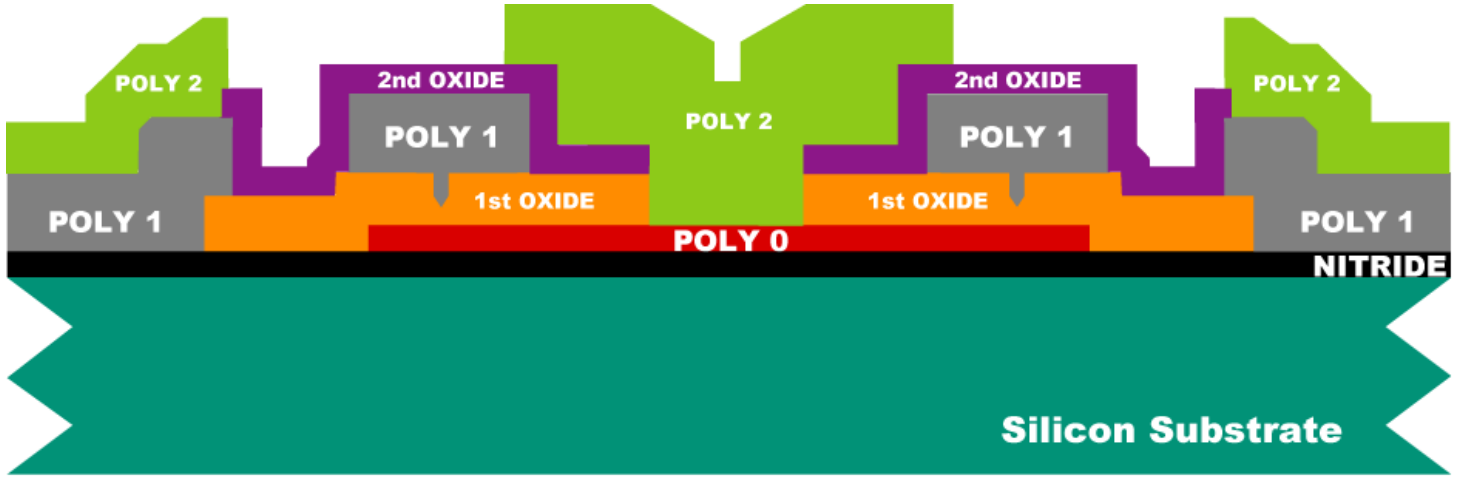
PolyMUMPs Process

- The second polysilicon layer is deposited followed by a thin PSG layer. The is annealed to reduce the poly 2 stress and dope the poly 2. Because the CVD film is conformal, all the holes will be filled, to varying degrees, with poly 2.



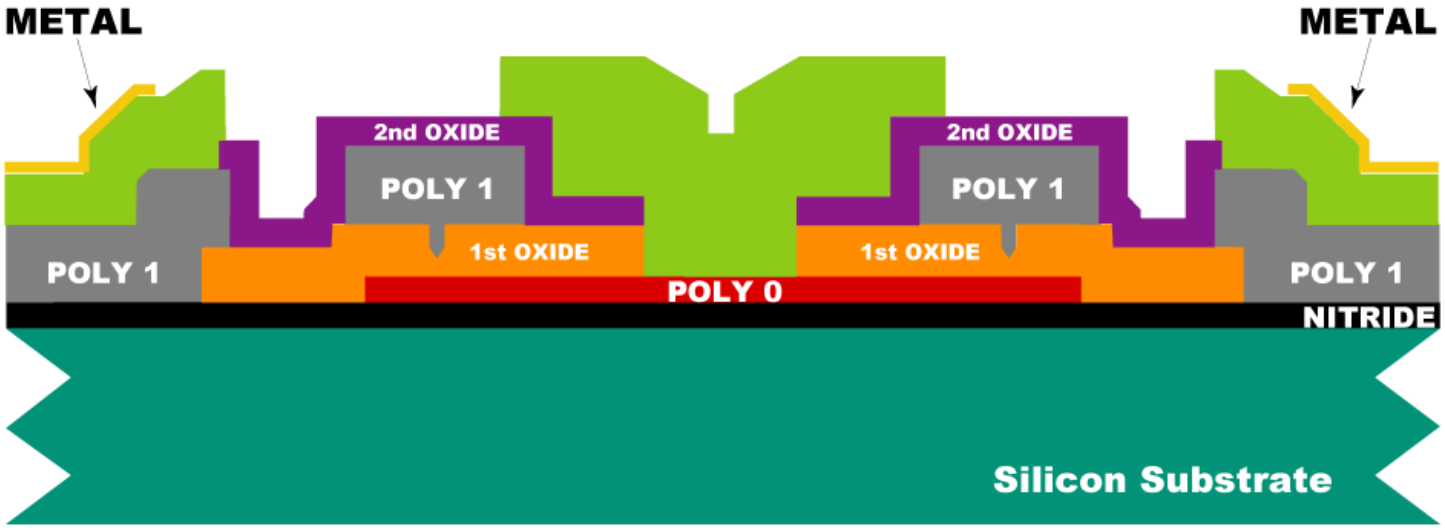
PolyMUMPs Process

- The wafer is coated with photoresist and the seventh mask (POLY2) is patterned. Both the photoresist and thin PSG (hard mask) will mask the RIE etch.
- After the poly 2 layer is etched and the wafer is stripped, the basic mechanical structure is complete



PolyMUMPs Process

- A lift-off template is used to deposit the metal layer (gold with a thin adhesion layer) on the wafer. Photoresist is patterned using the eighth (and ninth) masks (METAL) and the metal is deposited, adhering to the poly 2, where exposed, and breaking continuity as it goes over the photoresist step.
- The structure is now completed and ready for releasing.

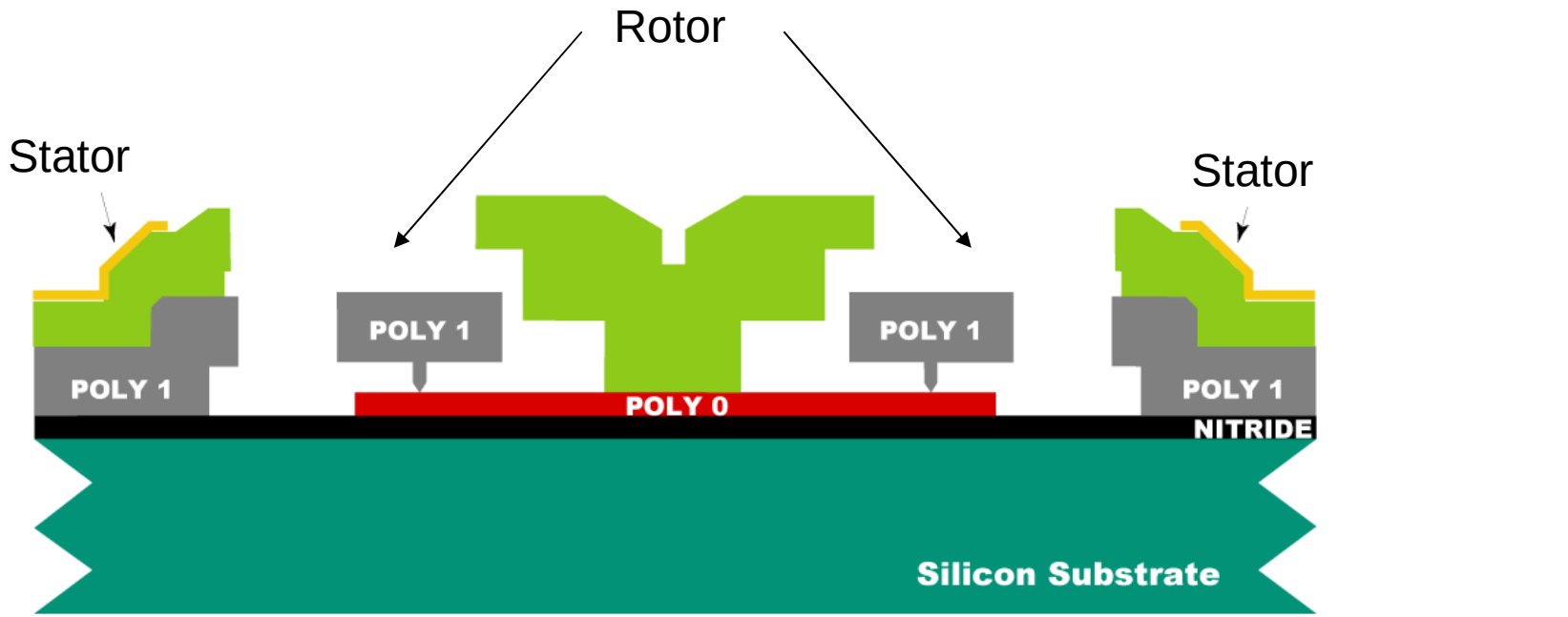


Release using Hydrofluoric Acid

- Remove the protective photoresist layer in a solvent bath
- Immerse chips in a bath of straight 49% HF at room temperature for 2.5 minutes to release the structures
- Rinse chips in DI water, followed by soaking in isopropyl alcohol and baking in a convection oven

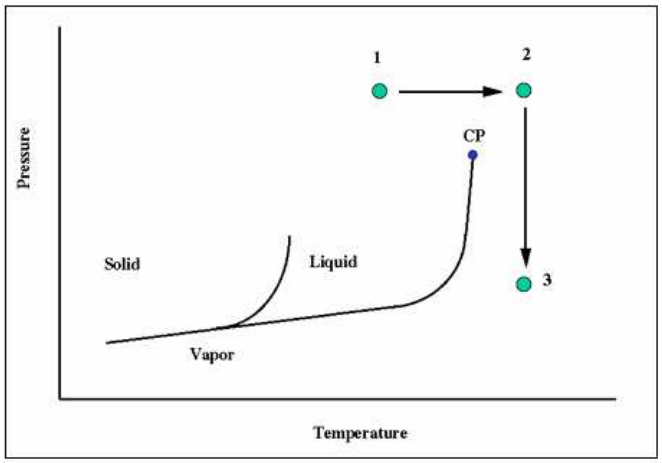
PolyMUMPs Process

- The wet etch removes all the sacrificial oxide layers and releases the moveable mechanical parts. The rotor is now free to spin about the center pin, and the stator poles are fixed and electrically active.



Dry using Supercritical CO_2 Drying

- Critical point drying circumvents surface tension effects by avoiding the liquid/vapor interface
  - CO_2 critical point is 31.1℃ and 1073 psi, allowing for room temperature procedure
  - Chips transferred to chamber in methanol (completely miscible in liquid CO_2)



Máscaras y reglas de diseño

Mnemonic Level Name	Field Type	Purpose
POLY0	light	pattern ground plane
ANCHOR1	dark	open holes for POLY1 to nitride or POLY0 connection
DIMPLE	dark	create dimples/bushings for POLY1
POLY1	light	pattern POLY1
POLY1_POLY2_VIA	dark	open holes for POLY1 to POLY2 connection
ANCHOR2	dark	open holes for POLY2 to nitride or POLY0 connection
POLY2	light	pattern POLY2
METAL	light	pattern METAL
HOLE0	dark	provide holes for POLY0
HOLE1	dark	provide release holes for POLY1
HOLE2	dark	provide release holes for POLY2
HOLEM	dark	provide release holes in METAL

Máscaras y reglas de diseño

Mnemonic Level Name	CIF Level Name	GDS Level #	Nominal Line Space	Min. Feature	Min. Space
*POLY0	CPZ	13	3.0	2.0	2.0
*ANCHOR1	COF	43	3.0	3.0	2.0
*DIMPLE	COS	50	3.0	2.0	3.0
*POLY1	CPS	45	3.0	2.05	2.0
*POLY1_POLY2_VIA	COT	47	3.0	2.0	2.0
*ANCHOR2	COL	52	3.0	3.0	2.0
*POLY2	CPT	49	3.0	2.05	2.0
*METAL	CCM	51	3.0	3.0	3.0
*HOLE0	CHZ	41	3.0	2.0	2.0
*HOLE1	CHO	0	3.0	3.0	3.0
*HOLE2	CHT	1	3.0	3.0	3.0
*HOLEM	CHM	48	4.0	4.0	4.0

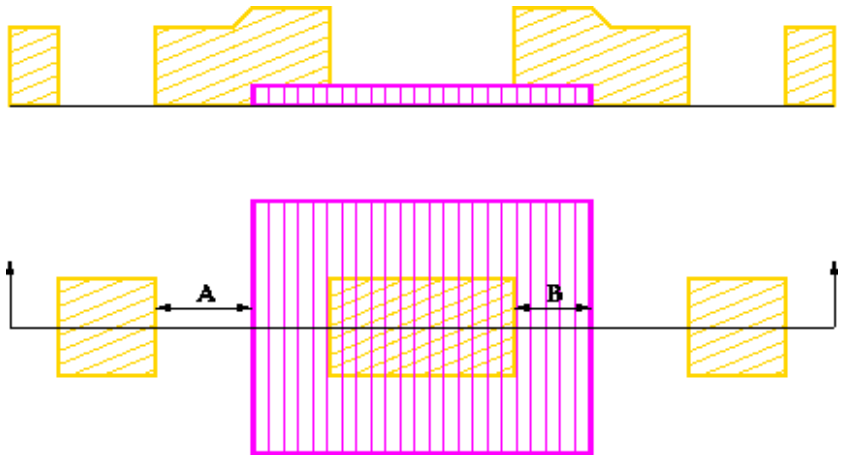
21 reglas de diseño

Rule	Rule Letter	Figure #	Min. Value (µm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0

Rule	Rule Letter	Figure #	Min. Value (µm)
POLY1 enclose ANCHOR1	G	2.6	4.0
POLY1 enclose DIMPLE	N	2.13	4.0
POLY1 enclose POLY1_POLY2_VIA	H	2.9, 2.11	4.0
POLY1 enclose POLY2	O	2.14	4.0
POLY1 space to ANCHOR2	K	2.11	3.0
*Lateral etch holes space in POLY1	R	2.15	=30 (max. value)

Rule	Rule Letter	Figure #	Min. Value (µm)
POLY2 enclose ANCHOR2	J	2.7, 2.10	5.0
POLY2 enclose POLY1_POLY2_VIA	L	2.9	4.0
POLY2 cut-in POLY1	P	2.14	5.0
POLY2 cut-out POLY1	Q	2.14	4.0
POLY2 enclose METAL	M	2.12	3.0
POLY2 space to POLY1	I	2.10	3.0
HOLE2 enclose HOLE1	T	2.16	2.0
HOLEM enclose HOLE2	U	2.16	2.0
*Lateral etch holes space in POLY2	S	2.15	=30 (max. value)

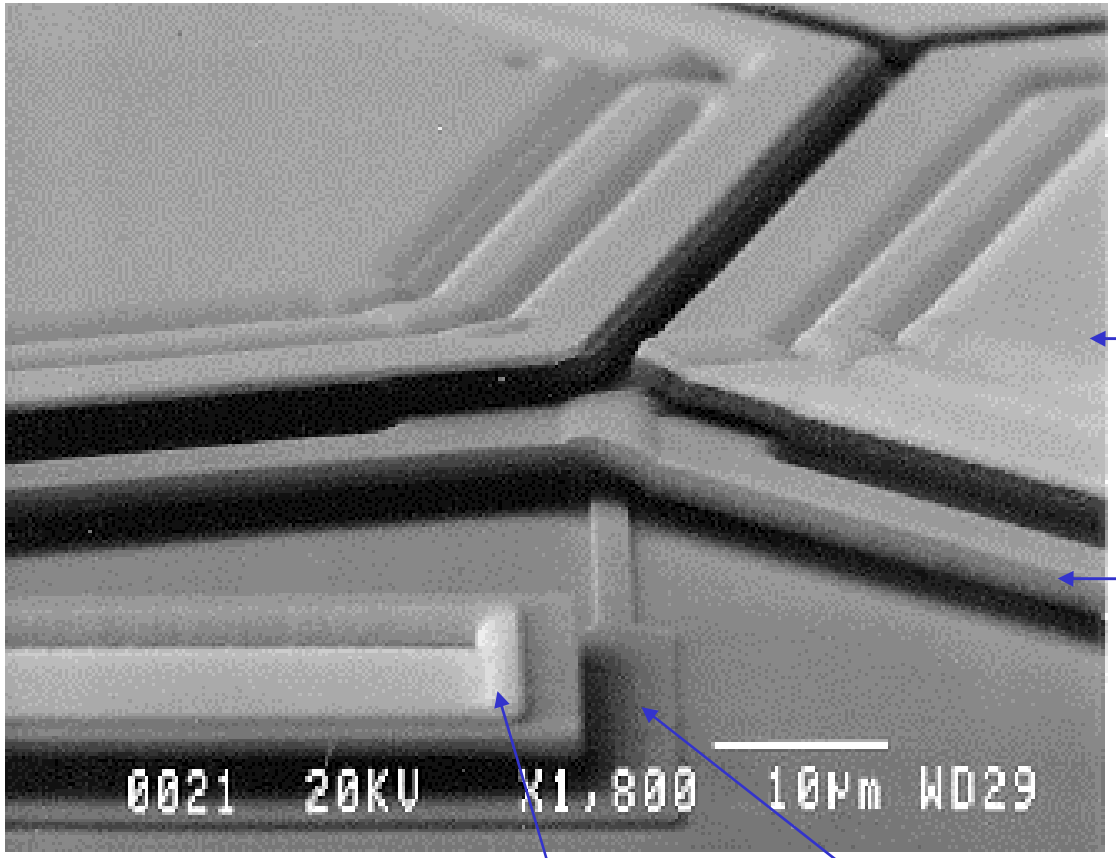
Ejemplo de regla de diseño



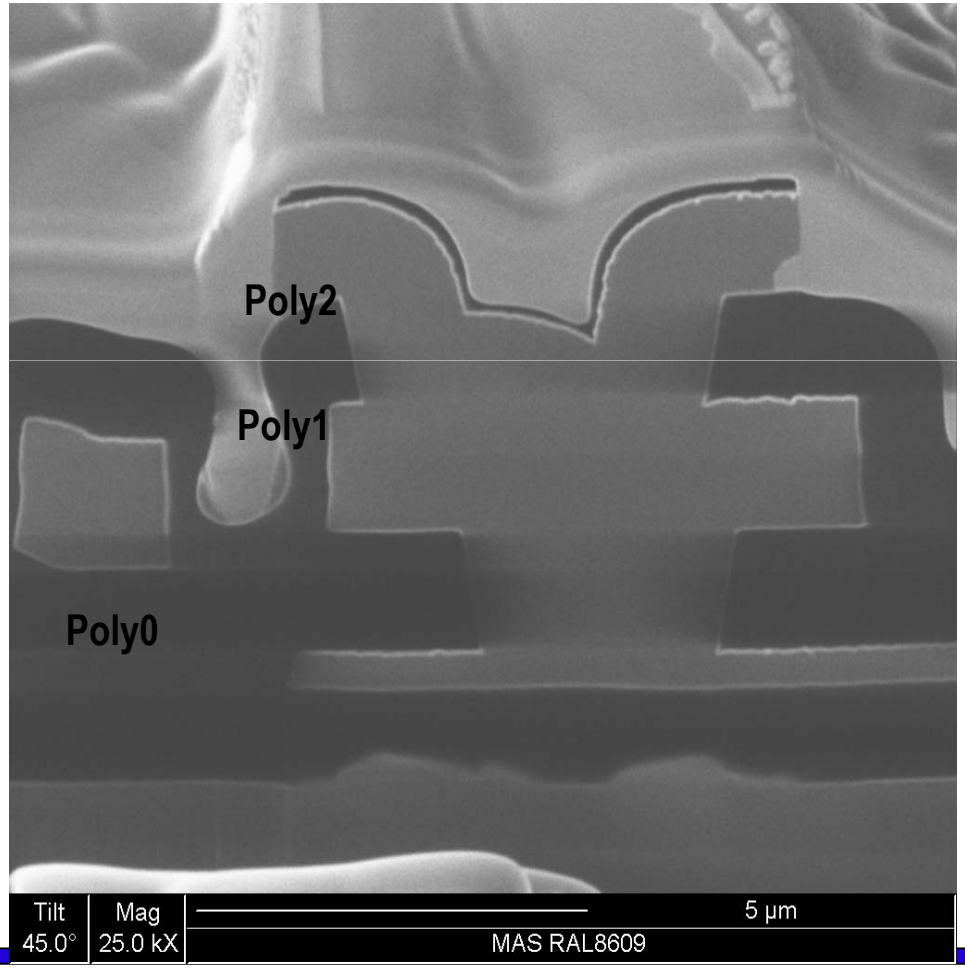
A: POLY0 space to ANCHOR1--4.0um The necessary separation between POLY0 and ANCHOR1 hole to ensure that POLY0 is not exposed.

B: POLY0 enclose ANCHOR1--4.0 um. The distance necessary between the edge of POLY0 and an ANCHOR1 hole to ensure the hole does not extend beyond the edge of POLY0.

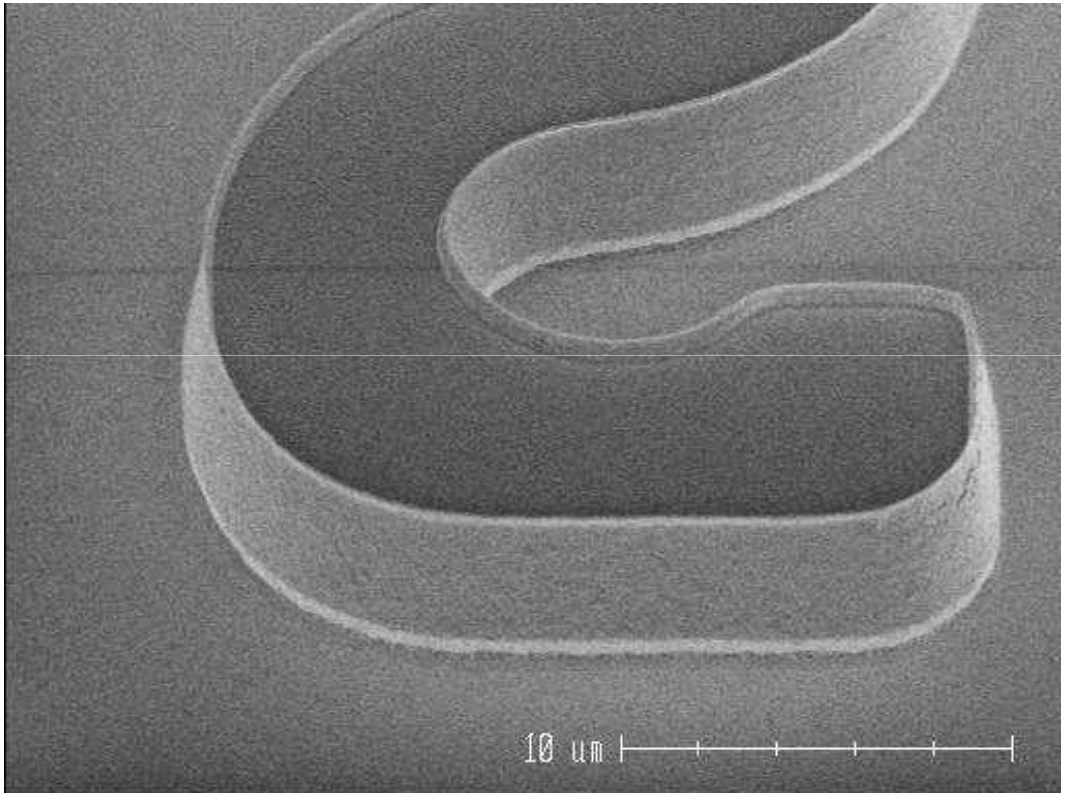
Resultado de las reglas de diseño



SEM Cross Section

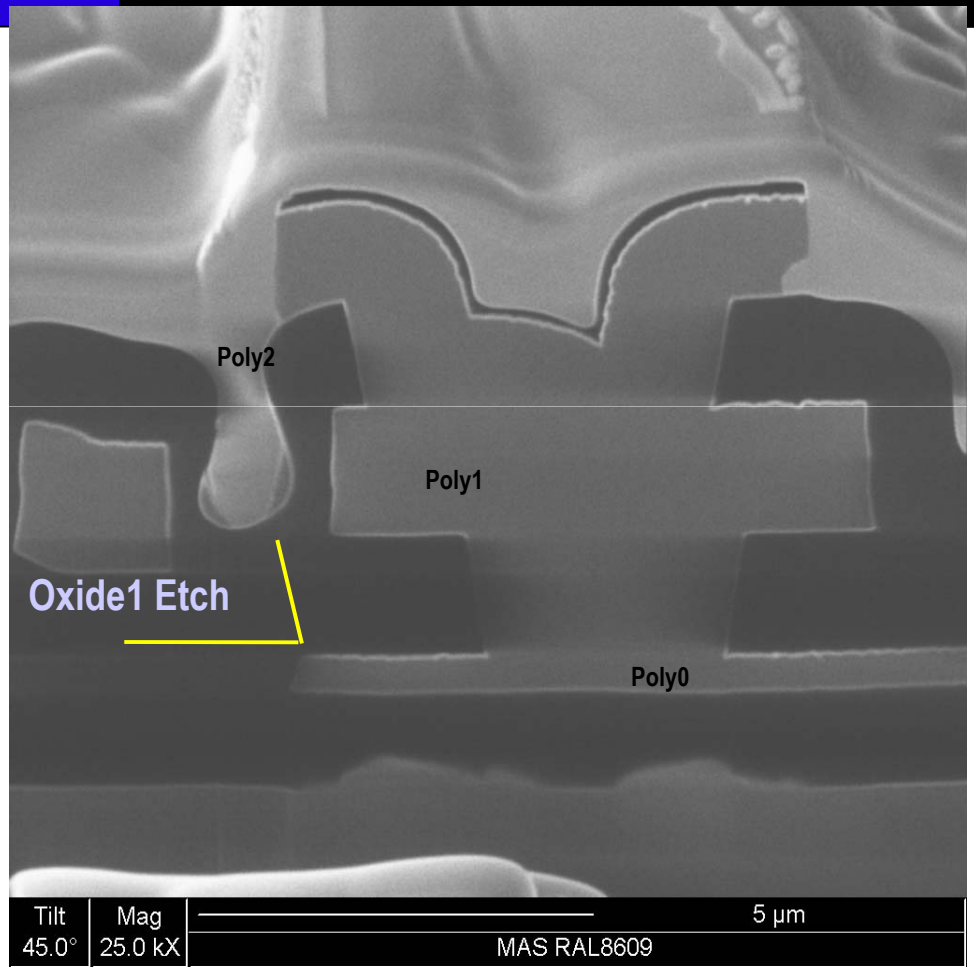


Poly Sidewalls

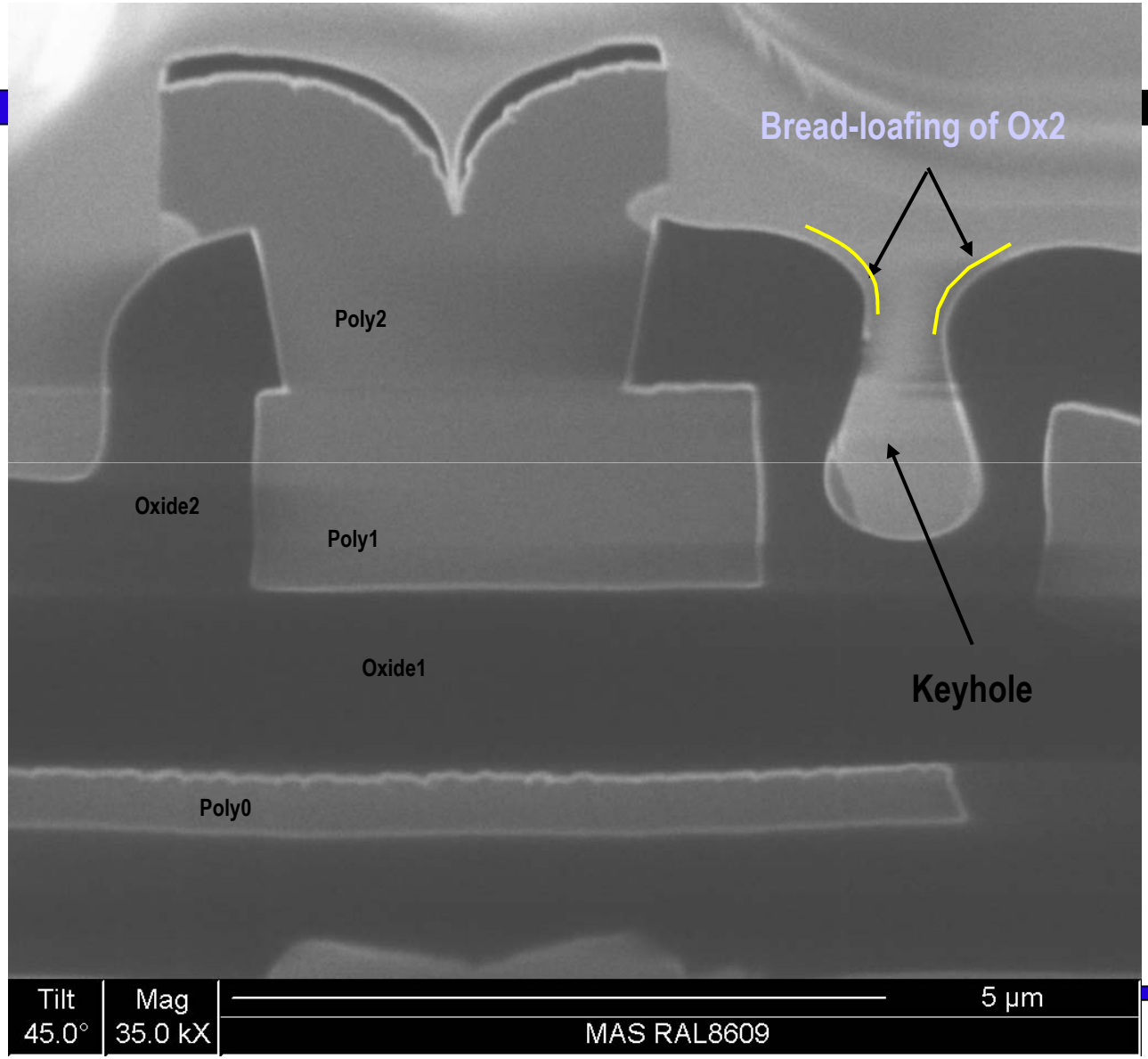


This is a 1um thick poly film. The thicker the poly the rougher the sidewall will be.

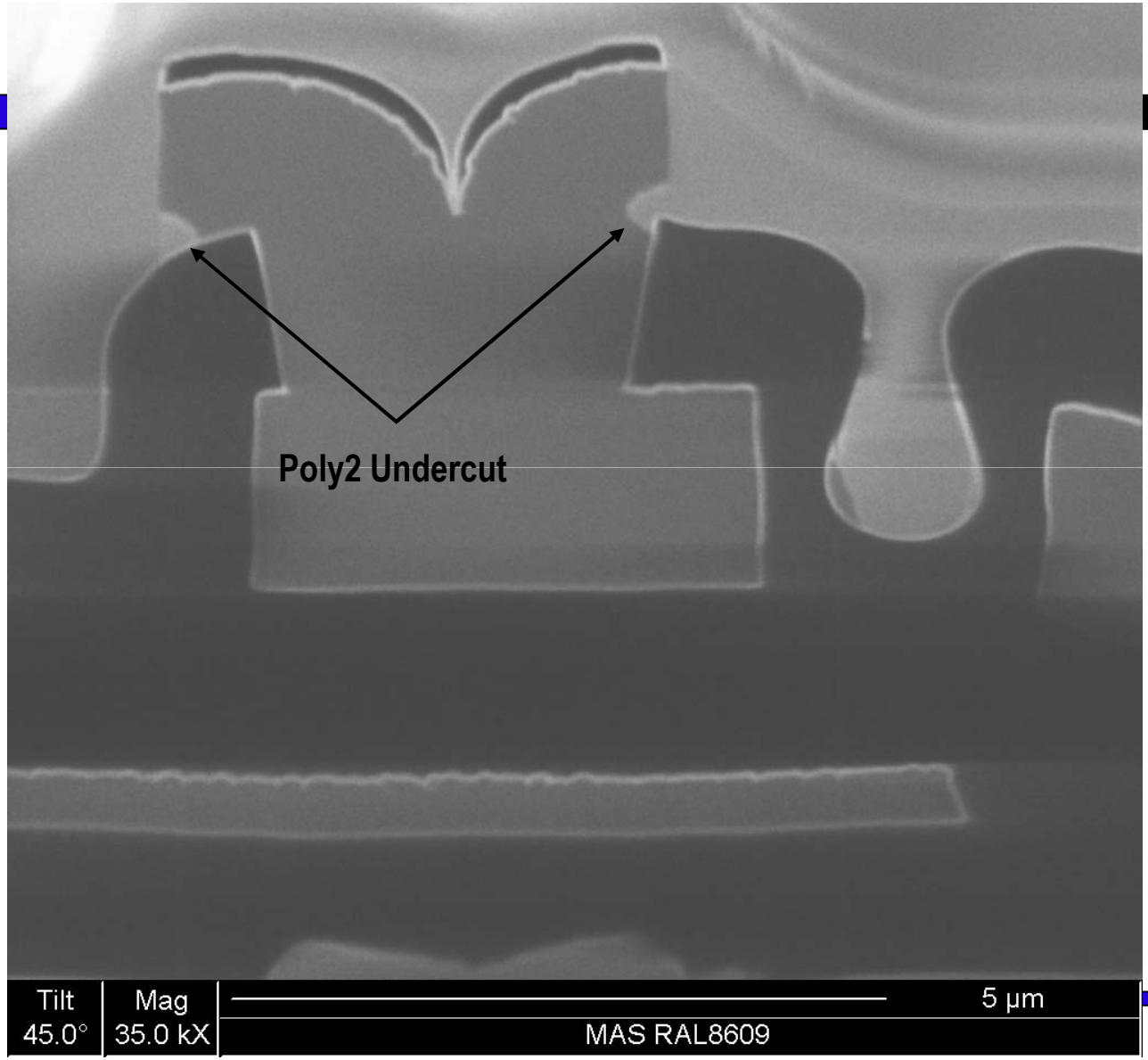
SEM Cross Section



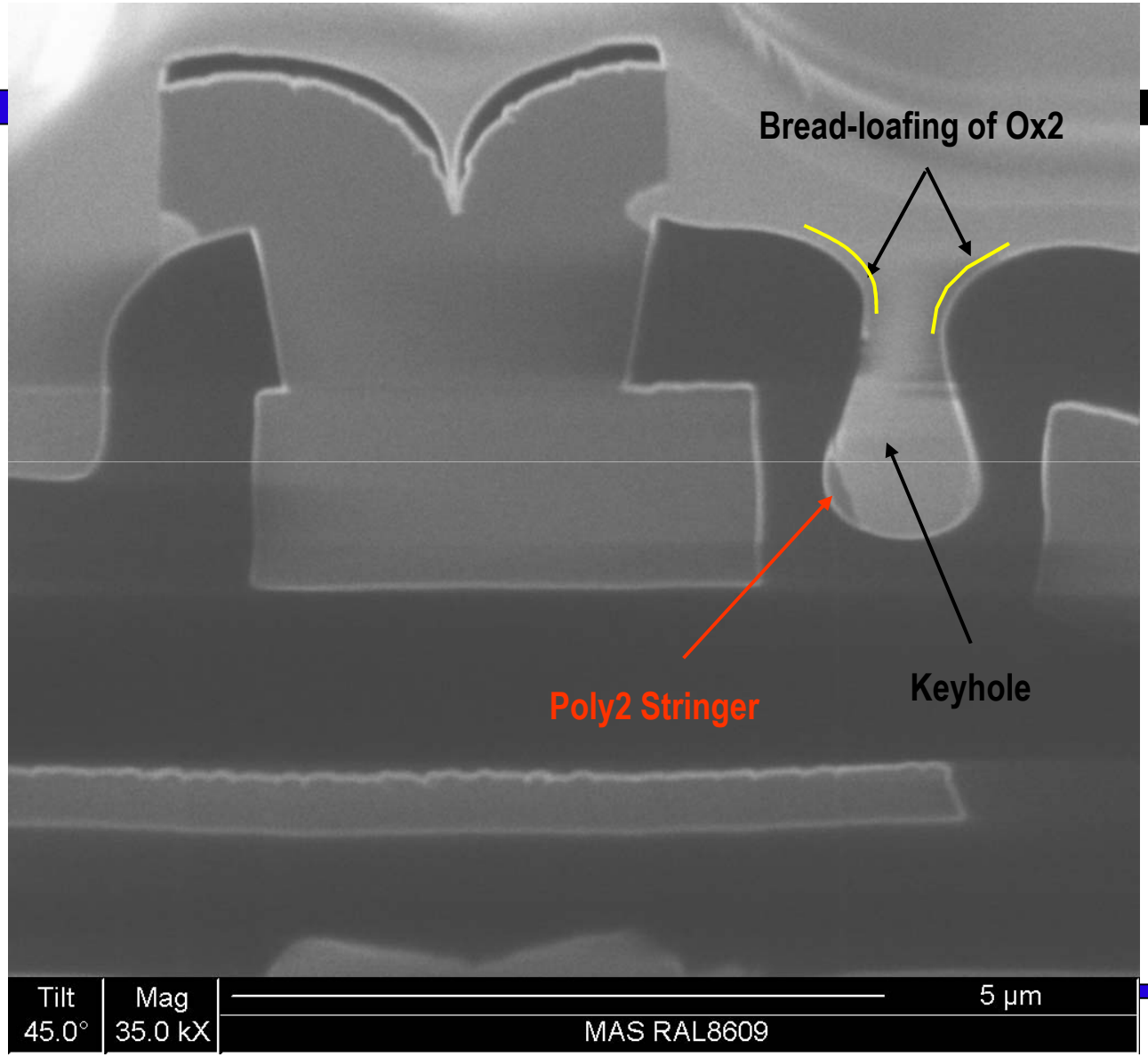
SEM Cross Section



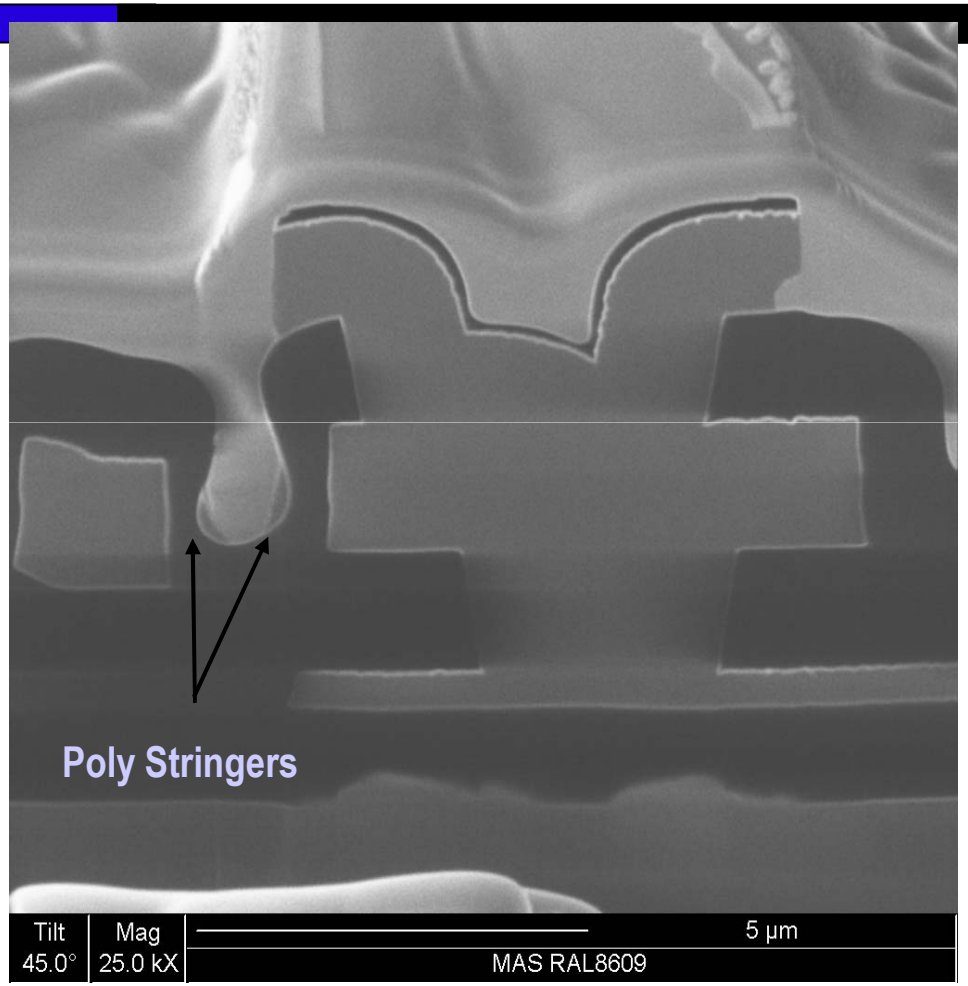
SEM Cross Section



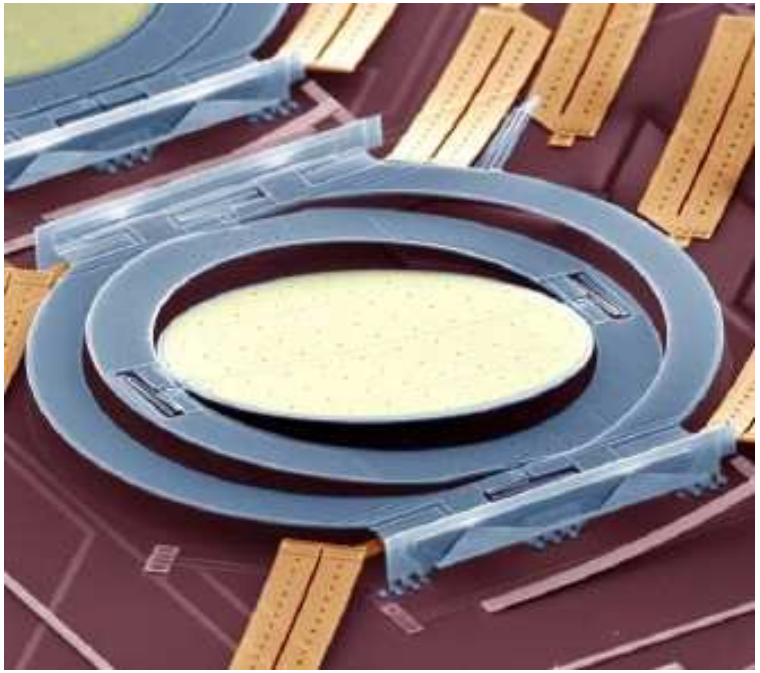
SEM Cross Section



SEM Cross Section



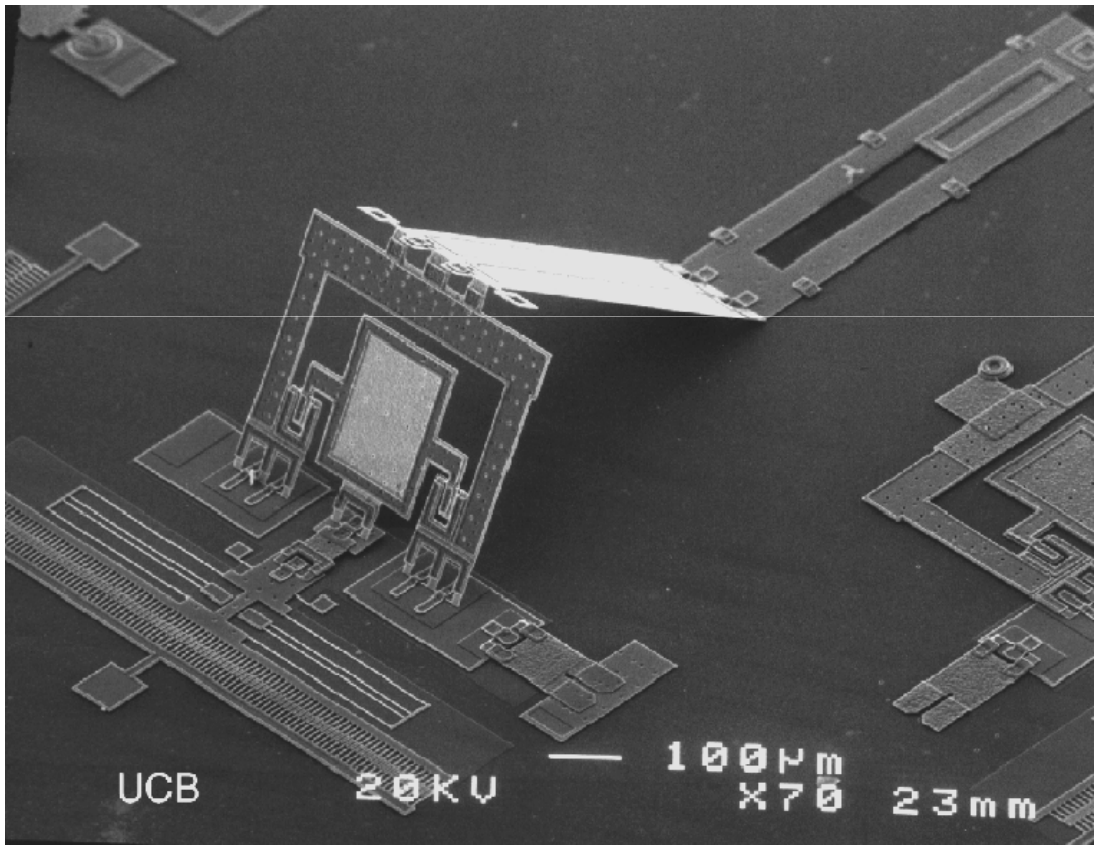
Ejemplos de dispositivos



Espejo

Bell Labs MEMS Team

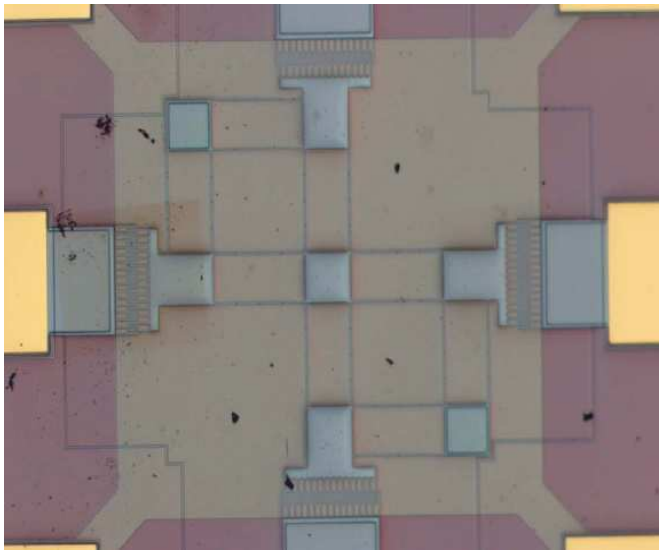
Ejemplos de dispositivos

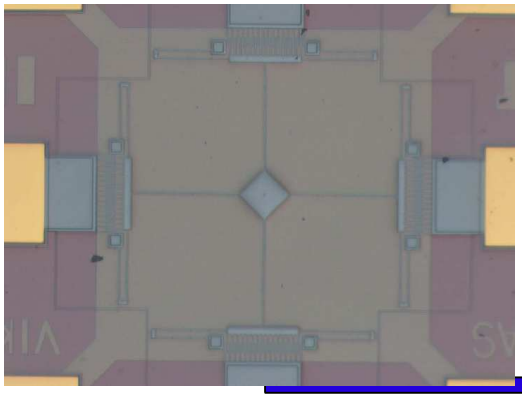


Espejo

UC Berkeley

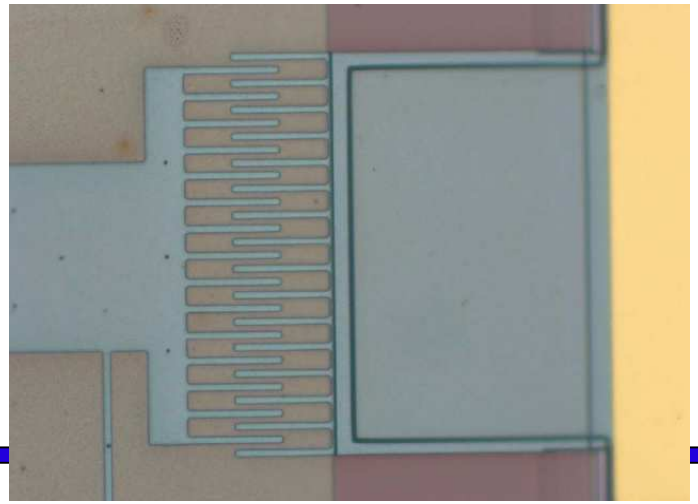
Ejemplos de dispositivos





Nanoposicionador

Univ. Colorado, Boulder



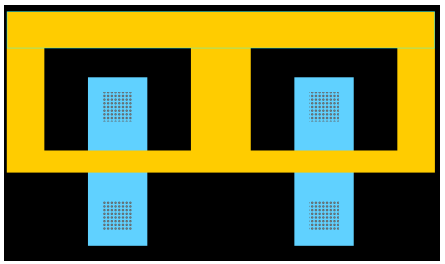
CaMEL

CaMEL (Consolidated Microelectromechanical Library) contains a non-parameterized cell database and a parameterized MEMS element library, for use by both the novice and advanced MEMS designers.

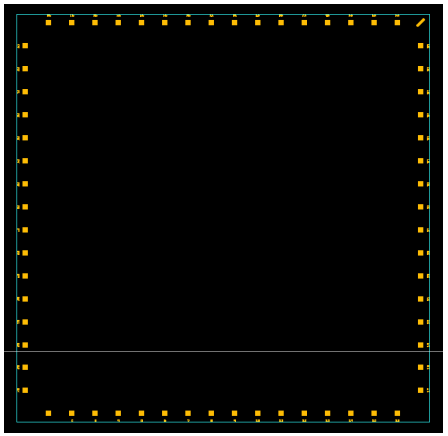
Both libraries are intended to assist users in the design and layout of MEMS devices by providing an initial layout for components of a MEMS system.

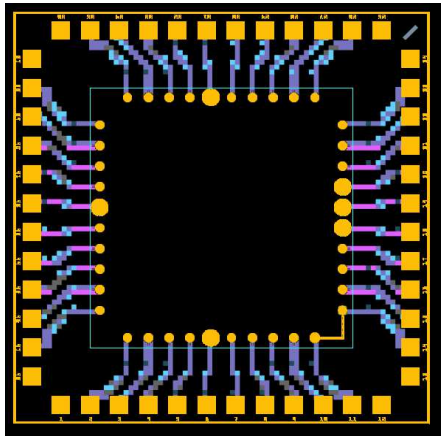
No longer supported by MemsCAP, but provided for free

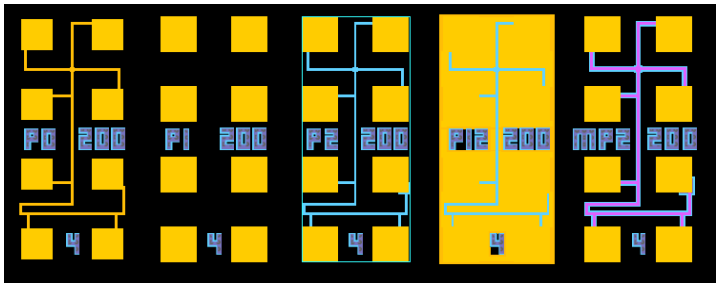
CaMEL



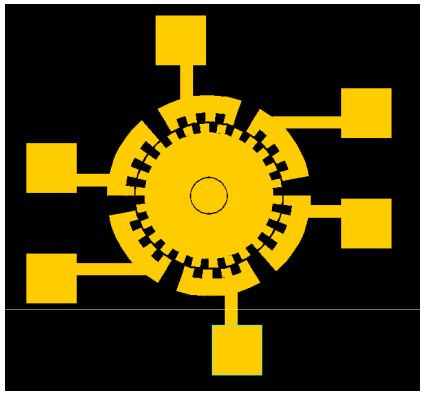
Hinges, test structures, pad frames

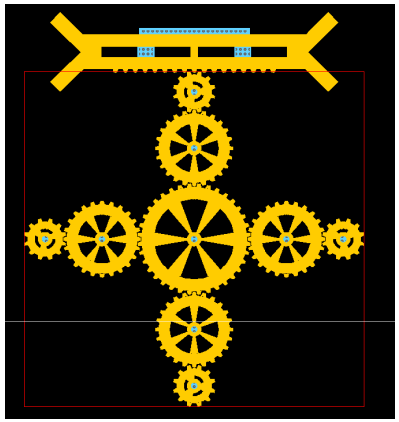


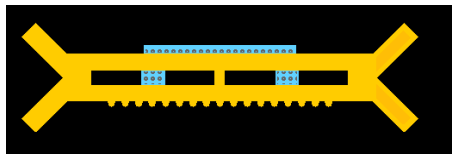


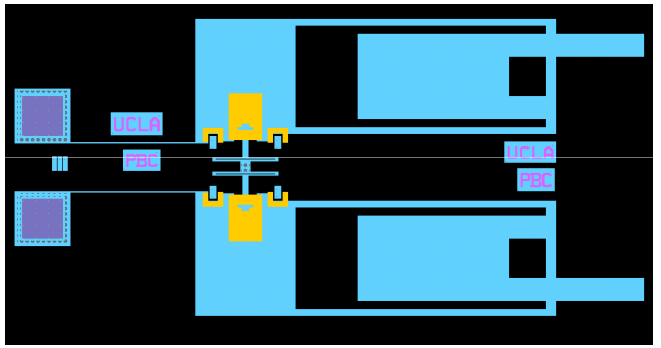


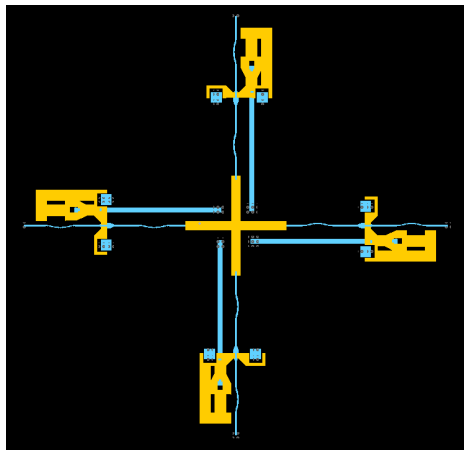
CaMEL

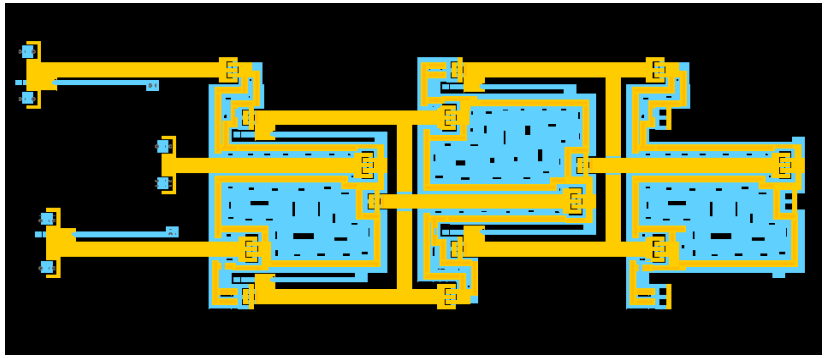












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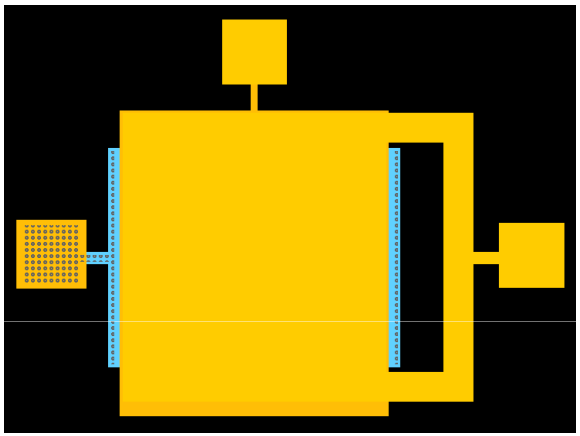

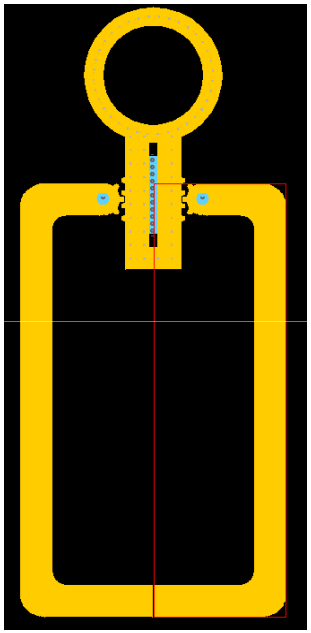

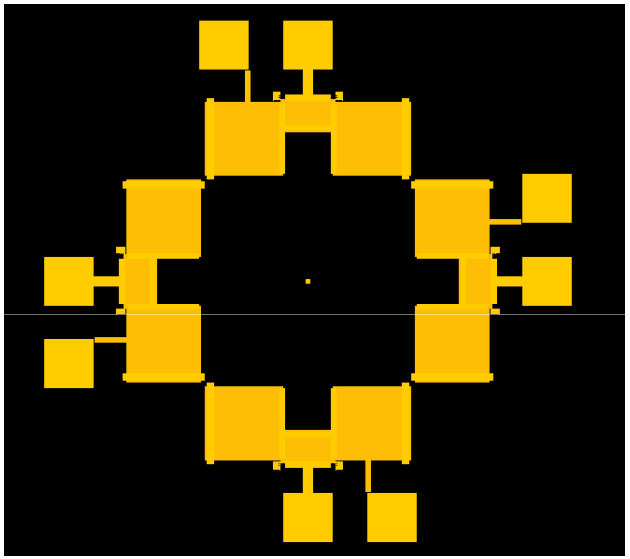

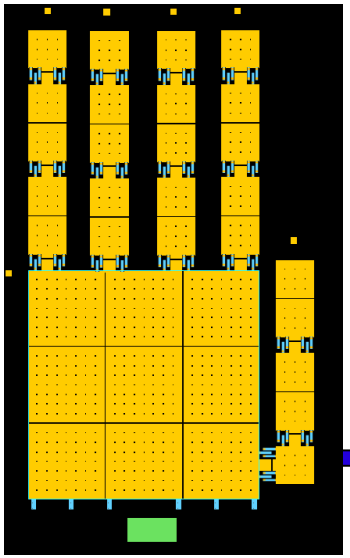

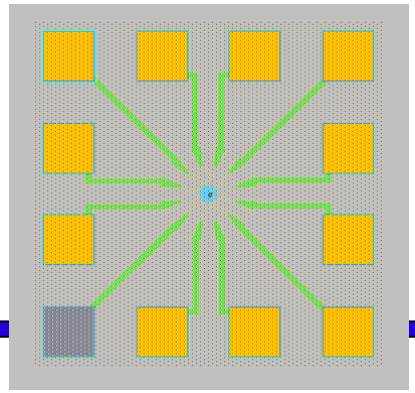

Coste y runs

MEMSCAP
The Power of a Small World™

MUMPs Price List		
PolyMUMPs	**Academic Rate**	**Non-Academic Rate**
1 Standard Die Site - 15 die delivered	$3,700	$5,300
1 Standard Die Site - 30 die delivered	$5,200	$6,800
1 Standard Die Site - 45 die delivered	$6,700	$8,300
Additional Standard Die Sites on same run	$2700/ea	$3100/ea
Saw Subdicing (per 15 die or subdie)	$200 for each cut	
HF Release (up to 60 die)*	$800	
HF Release and CO2 Dry (up to 60 die)*	$1,800	
PolyMUMPs NOTES		
"Standard Die Site" is a 10mm x 10mm design/die space with 15 unreleased die shipped		
*From Same Die Site/Design		

MEMSCAP
The Power of a Small World™

2011-2012 MUMPs Run Schedule

Run	Design Deadline	Std Ship Date
MetalMUMPs Run 28	Tue-Sep-20-2011	Thu-Dec-01-2011
MetalMUMPs Run 29	Tue-Mar-13-2012	Thu-May-24-2012
MetalMUMPs Run 30	Tue-Sep-18-2012	Tue-Dec-04-2012
PolyMUMPs Run 97	Tue-Oct-11-2011	Mon-Dec-12-2011
PolyMUMPs Run 98	Tue-Jan-17-2012	Fri-Mar-16-2012
PolyMUMPs Run 99	Tue-Apr-10-2012	Tue-Jun-12-2012
PolyMUMPs Run 100	Wed-Jul-04-2012	Mon-Sep-10-2012
PolyMUMPs Run 101	Tue-Oct-09-2012	Thu-Dec-13-2012
SOIMUMPs Run 37	Tue-Oct-25-2011	Thu-Dec-15-2011
SOIMUMPs Run 38	Tue-Jan-10-2012	Thu-Mar-01-2012
SOIMUMPs Run 39	Tue-Apr-03-2012	Wed-May-30-2012
SOIMUMPs Run 40	Tue-Jun-26-2012	Tue-Aug-21-2012
SOIMUMPs Run 41	Tue-Sep-18-2012	Wed-Nov-14-2012

http://www.memscap.com